AMENDMENTS

In the Claims:

These claims replace all prior versions and listings of claims in the above-referenced application.

1-15. (Canceled)

16. (New) An apparatus comprising:

a multiply accumulate (MAC) unit coupled to operand busses at respective operand inputs, the MAC unit configured to latch a first multiple-bit data value during a first cycle and execute the MAC functions on the first multiple-bit data value during the next subsequent cycle while latching a second multiple-bit data value, the MAC unit further configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus once the first MAC result is available and latch a second MAC result responsive to the second multiple-bit data value;

a register coupled to the result bus and configured to latch the first MAC result; and

a miscellaneous logic unit coupled between the result bus and the register, the miscellaneous logic unit configured to generate first and second control signals responsive to at least one certain exceptional condition, wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus, when the second control signal is asserted the first MAC result is driven from the register onto the result bus, and wherein when the second control signal is not asserted a miscellaneous-unit generated result is driven onto the result bus.

17. (New) The apparatus of claim 16, wherein the miscellaneous logic unit is configured to identify and exceptional condition responsive to an operand.

18. (New) The apparatus of claim 16, wherein the miscellaneous logic unit is configured to recognize an exceptional condition identified by the MAC unit.

19. (New) The apparatus of claim 18, wherein the miscellaneous logic unit directs the replacement of one of the first and second MAC results with a representation of the exceptional condition.

20. (New) A method for performing single-instruction multiple-data instructions comprising:

applying a plurality of data values on an operand bus for two consecutive cycles;

latching a first data value in a multiply accumulate (MAC) unit during a first cycle;

initiating execution of the multiply and accumulate functions on the first data value and latching a second data value in the MAC unit during a second cycle;

deferring a first MAC unit result responsive to the first data value;

initiating execution of the multiply and accumulate functions on the second data value during a cycle subsequent to the second cycle to generate a second MAC unit result; and

generating a plurality of control signals responsive to the first data value, the second data value, and an exceptional condition when identified by the MAC unit.

21. (New) The method of claim 20, further comprising applying the plurality of control signals to arrange a combination selected from the first MAC unit result, the second MAC unit result, and a representation of an exceptional condition.

22. (New) The method of claim 20, wherein deferring comprises forwarding the first MAC unit result to a register.

23. (New) The method of claim 20, wherein generating comprises determining when an operand is invalid.

24. (New) The method of claim 20, wherein generating comprises determining when an operation in combination with an operand will produce an exceptional condition.

25. (New) The method of claim 20, further comprising forwarding the combination to a result bus.

26. (New) An apparatus comprising:

means for producing a plurality of control signals responsive to a first data value, a second data value, and an exceptional condition, wherein the exception condition results from the execution of a multiply accumulate (MAC) unit over the first and second data values; and

means for arranging a combination selected from a first MAC unit result, a second MAC unit result, and a representation of the exceptional condition responsive to the plurality of control signals.

27. (New) The apparatus of claim 26, wherein the first MAC unit result is responsive to the first data value.

28. (New) The apparatus of claim 26, wherein the second MAC unit result is responsive to the second data value.

29. (New) The apparatus of claim 26, wherein the exceptional condition is identified by the MAC unit.

30. (New) The apparatus of claim 26, wherein the exceptional condition is identified by the means for producing the plurality of control signals responsive to at least one of the first and second data values and an opcode.